UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,426	12/07/2001	Daniel M. Castagnozzi	applied_114	9539

29397 7590 07/13/2005

LAW OFFICE OF GERALD MALISZEWSKI
P.O. BOX 270829
SAN DIEGO, CA 92198-2829

EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,426	CASTAGNOZZI ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 17, 33 and 35 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 17-48 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The preamble of claims 17 and 33 recite, "A non-causal channel equalization communication system". The omitted elements are: the relationship between "channel equalization communication system" and the body of the claims.

The Examiner would like to point out that it is not clear what connection the multi-threshold circuit and the non-causal circuit have to "non-causal channel equalization communication system" in general and specifically to do with equalization recited in the preamble.

The preamble of claim 35 recites, "A non-causal channel equalization communication system". The omitted elements are: the relationship between "channel equalization communication system" and the body of the claims.

The Examiner would like to point out that it is not clear what connection the multi-threshold circuit, the non-causal circuit and the forward error correction circuit have to do with "non-causal channel equalization communication system" in general and specifically to equalization recited in the preamble.

Claim 17 recites "each NRZ data" in line 5. There is no antecedent basis for "each NRZ data" and it is not clear what the relationship between "each NRZ data" and a "NRZ data **stream**" [Emphasis Added] in line 4 is.

Claim 33 recites "each data" in lines 4-5. There is no antecedent basis for "each data" and it is not clear what the relationship between "each data" and a "data **stream**" [Emphasis Added] in line 4 is.

Claim 35 recites "each data" in line 5. There is no antecedent basis for "each data" and it is not clear what the relationship between "each data" and a "data **stream**" [Emphasis Added] in line 4 is.

The Examiner would like to point out that the body of claims 17, 33 and 35 substantially claim a circuit using threshold values for updating bit estimates. A valid search for claims 17, 33 and 35 must include the following EAST search: (threshold ((upper lower) adj bound)) and ((bit adj estimate) sample quantize quantized quantizing quantizes) and (clock cycle period) and ((threshold ((upper lower) adj bound)) with (compare compares comparing compared comparison match matches matching matched)) which produces 27,493 patent literature documents. The Examiner has not even mentioned the additional class searches that the Examiner must make. The Examiner would like to

point out that not only is such a search an undue burden on the Examiner since EAST will only pull 2000 documents at a time, the complete search is impossible. The Examiner makes this of record, so that if the Examiner does become frustrated with search and the amount of work necessary to complete a search in this area and decides to allow the case out of frustration, the courts will be apprised of the Examiners limitations. The Examiner asserts that even if the Examiner allowed the case out of frustration, there is no way the Examiner could guarantee the validity of claims 17, 33 and 35, as written, due to the broadness an indefiniteness of the claim language. The Examiner recommends that the applicant modify the claims to more closely claim what the Applicant considers as his invention so that the Examiner can conclude a search without undue burden, that is, if the Applicant is interested in a valid patent (Note: the applicant only teaches the body of the claims 17, 33 and 35 in an equalization unit, which is not reflected in the body of the claims).

Claims 17-48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 17 recites "each NRZ data" in line 5. There is no antecedent basis for "each NRZ data" and it is not clear what the relationship between "each NRZ data" and a "NRZ data stream" [Emphasis Added] in line 4 is.

Claim 33 recites "each data" in lines 4-5. There is no antecedent basis for "each data" and it is not clear what the relationship between "each data" and a "data **stream**" [Emphasis Added] in line 4 is.

Claim 33 recites "each data" in line 5. There is no antecedent basis for "each data" and it is not clear what the relationship between "each data" and a "data **stream**" [Emphasis Added] in line 4 is.

The preamble of claims 17, 33 and 35 recite, "A non-causal channel equalization communication system". The Examiner would like to point out that equalization applies to received data and is generally implement in a receiver. A communication system includes a transmitter. It is not clear how equalization applies to the transmitter or how nay of the elements of the body of claims 17, 33 and 35 can be associated with a transmitter. The Examiner believes the applicant intended --A non-causal channel equalization unit for a receiver in a communication system--.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 33 is rejected under 35 U.S.C. 102(b) as being anticipated by Andresen; Rolf et al. (US 3670304 A).

35 U.S.C. 103(a) rejection of claim 33.

Andresen teaches a multi-threshold decision circuit having an input to accept a data stream encoded with forward error correction FEC (Amplitude Sense and Data Gates 20 in Figures 1 & 3 in Andresen are a multi-threshold decision circuit having an input to accept a data stream encoded with forward error correction FEC), an input to accept threshold values (Input Line 44 in Figure 1 of Andresen provides a Change Threshold value to Amplitude Sense and Data Gates 20), and outputs to provide bit estimates responsive to a plurality of voltage threshold levels (Output Lines 27 and 72 in Figures 1 & 3 of Andresen provide bit estimates responsive to a plurality of voltage threshold levels); a non-casual circuit having inputs to accept bit estimates from the multi-threshold decision circuit (Data/Error Detectors in Figures 1 & 3 of Andresen are a non-causal circuit having inputs to accept bit estimates from the Amplitude Sense and Data Gates multi-threshold decision circuit 20), the non-casual circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles (non-casual circuit Data/Error Detectors in Figures 1 & 3 of Andresen comprise Data Detector 28 in Figure 1 & 6 comprising Comparators 124 & 138 in Figure 6 for comparing a current bit estimate D in Figures 6 & 7 to bit value reference decisions R1 and R2 made across a plurality of clock cycles; Note: bit value reference decisions R1 and R2 are predetermined reference values made across a plurality of clock cycles); the non-casual circuit having an output to supply a bit value for the current bit estimate determined in response to the non-casual bit value comparisons (Data Detector 28 inside the non-casual circuit Data/Error Detectors 24 in Figures 1 & 3 of Andresen

supplies a Data output which is the current bit estimate determined in response to the non-casual bit value comparisons); a forward error correction FEC circuit having an input to receive the first bit value from the non-casual circuit (Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen are an FEC circuit having an input to receive a first bit value from the non-casual circuit Data/Error Detectors 24), the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen decode and correct the incoming data stream), the FEC circuit having an output to supply a stream of corrected data bits (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen have an output to supply the Read Data stream of corrected data bits); and, a statistics circuit having an input to accept the first bit value from the non-casual circuit, an input to accept the stream of corrected data bits from the FEC circuit, and an output to supply threshold values to the multi-threshold circuit in response to analysis of the FEC error statistics (Check Change Threshold Circuits 26, 90 and 92 in Figures 1 & 3 of Andresen are a statistics circuit having an input to accept the first bit value from the non-casual circuit Data/Error Detectors 24, an input to accept the stream of corrected data bits from the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96, and an output to supply threshold values to the multi-threshold circuit Amplitude Sense and Data Gates 20 in Figures 1 & 3 in response to analysis of the FEC error statistics).

The Examiner asserts that Exclusive OR circuit 112 in Figure 6 of Andresen is substantially a comparator since it provides a 1 if input signal match and a 0 if they do

not match. Exclusive OR circuit 112 in Figure 6 receives a current bit estimate A and a previous bit estimate A from Delay 110 in Figure 6. Previous bit estimate A from Delay 110 in Figure 6 is a bit value for a non-current clock cycle. Hence Andresen teaches an output DATA in Figure 1 of Andresen to supply a first bit value for a current clock cycle in response to comparing a first bit estimate A for the current clock cycle, to bit values determined A from Delay 110 in Figure 6 in a non-current clock cycle (Note Figure 6 is the Data Detector 28 of Figure 1 in Andresen).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Andresen; Rolf et al. (US 3670304 A) in view of The Authoritative Dictionary of IEEE

Standards Terms (The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, page 742).

35 U.S.C. 103(a) rejection of claim 17.

Andresen teaches a multi-threshold decision circuit having an input to accept a data stream encoded with forward error correction FEC (Amplitude Sense and Data Gates 20 in Figures 1 & 3 in Andresen are a multi-threshold decision circuit having an input to accept a data stream encoded with forward error correction FEC), an input to accept threshold values (Input Line 44 in Figure 1 of Andresen provides a Change Threshold value to Amplitude Sense and Data Gates 20), and outputs to provide bit estimates responsive to a plurality of voltage threshold levels (Output Lines 27 and 72 in Figures 1 & 3 of Andresen provide bit estimates responsive to a plurality of voltage threshold levels); a non-casual circuit having inputs to accept bit estimates from the multi-threshold decision circuit (Data/Error Detectors in Figures 1 & 3 of Andresen are a non-causal circuit having inputs to accept bit estimates from the Amplitude Sense and Data Gates multi-threshold decision circuit 20), the non-casual circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles (non-casual circuit Data/Error Detectors in Figures 1 & 3 of Andresen comprise Data Detector 28 in Figure 1 & 6 comprising Comparators 124 & 138 in Figure 6 for comparing a current bit estimate D in Figures 6 & 7 to bit value reference decisions R1 and R2 made across a plurality of clock cycles; Note: bit value reference decisions R1 and R2 are predetermined reference values made across a plurality of clock cycles); the

non-casual circuit having an output to supply a bit value for the current bit estimate determined in response to the non-casual bit value comparisons (Data Detector 28 inside the non-casual circuit Data/Error Detectors 24 in Figures 1 & 3 of Andresen supplies a Data output which is the current bit estimate determined in response to the non-casual bit value comparisons); a forward error correction FEC circuit having an input to receive the first bit value from the non-casual circuit (Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen are an FEC circuit having an input to receive a first bit value from the non-casual circuit Data/Error Detectors 24), the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen decode and correct the incoming data stream), the FEC circuit having an output to supply a stream of corrected data bits (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen have an output to supply the Read Data stream of corrected data bits); and, a statistics circuit having an input to accept the first bit value from the non-casual circuit, an input to accept the stream of corrected data bits from the FEC circuit, and an output to supply threshold values to the multi-threshold circuit in response to analysis of the FEC error statistics (Check Change Threshold Circuits 26, 90 and 92 in Figures 1 & 3 of Andresen are a statistics circuit having an input to accept the first bit value from the non-casual circuit Data/Error Detectors 24, an input to accept the stream of corrected data bits from the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96, and an output to supply threshold values to the multi-threshold circuit Amplitude Sense and Data Gates

20 in Figures 1 & 3 in response to analysis of the FEC error statistics).

The Examiner asserts that Exclusive OR circuit 112 in Figure 6 of Andresen is substantially a comparator since it provides a 1 if input signal match and a 0 if they do not match. Exclusive OR circuit 112 in Figure 6 receives a current bit estimate A and a previous bit estimate A from Delay 110 in Figure 6. Previous bit estimate A from Delay 110 in Figure 6 is a bit value for a non-current clock cycle. Hence Andresen teaches an output DATA in Figure 1 of Andresen to supply a first bit value for a current clock cycle in response to comparing a first bit estimate A for the current clock cycle, to bit values determined A from Delay 110 in Figure 6 in a non-current clock cycle (Note Figure 6 is the Data Detector 28 of Figure 1 in Andresen).

However Andresen does not explicitly teach the specific use of non-return to zero NRZ. The Authoritative Dictionary of IEEE Standards Terms defines NRZ as a modulation technique for magnetic tape as taught in Andresen. The Examiner would like to point out that NRZ is a modulation technique to improve readability of a magnetic medium. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Andresen with the teachings of The Authoritative Dictionary of IEEE Standards Terms by including use of non-return to zero NRZ. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of non-return to zero NRZ would have improved readability of a magnetic medium.

5. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Andresen; Rolf et al. (US 3670304 A) and The Authoritative Dictionary of IEEE Standards Terms (The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, page 742) in view of Abe; Katsuaki et al. (US 5781588 A, hereafter referred to as Owaki).

35 U.S.C. 103(a) rejection of claim 35.

Andresen teaches a multi-threshold decision circuit having an input to accept a data stream encoded with forward error correction FEC (Amplitude Sense and Data Gates 20 in Figures 1 & 3 in Andresen are a multi-threshold decision circuit having an input to accept a data stream encoded with forward error correction FEC), an input to accept threshold values (Input Line 44 in Figure 1 of Andresen provides a Change Threshold value to Amplitude Sense and Data Gates 20), and outputs to provide bit estimates responsive to a plurality of voltage threshold levels (Output Lines 27 and 72 in Figures 1 & 3 of Andresen provide bit estimates responsive to a plurality of voltage threshold levels); a non-casual circuit having inputs to accept bit estimates from the multi-threshold decision circuit (Data/Error Detectors in Figures 1 & 3 of Andresen are a non-causal circuit having inputs to accept bit estimates from the Amplitude Sense and Data Gates multi-threshold decision circuit 20), the non-casual circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles (non-casual circuit Data/Error Detectors in Figures 1 & 3 of Andresen comprise Data Detector 28 in Figure 1 & 6 comprising Comparators 124 & 138 in Figure 6 for

comparing a current bit estimate D in Figures 6 & 7 to bit value reference decisions R1 and R2 made across a plurality of clock cycles; Note: bit value reference decisions R1 and R2 are predetermined reference values made across a plurality of clock cycles); the non-casual circuit having an output to supply a bit value for the current bit estimate determined in response to the non-casual bit value comparisons (Data Detector 28 inside the non-casual circuit Data/Error Detectors 24 in Figures 1 & 3 of Andresen supplies a Data output which is the current bit estimate determined in response to the non-casual bit value comparisons); a forward error correction FEC circuit having an input to receive the first bit value from the non-casual circuit (Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen are an FEC circuit having an input to receive a first bit value from the non-casual circuit Data/Error Detectors 24), the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen decode and correct the incoming data stream), the FEC circuit having an output to supply a stream of corrected data bits (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen have an output to supply the Read Data stream of corrected data bits); and, a statistics circuit having an input to accept the first bit value from the non-casual circuit, an input to accept the stream of corrected data bits from the FEC circuit, and an output to supply threshold values to the multi-threshold circuit in response to analysis of the FEC error statistics (Check Change Threshold Circuits 26, 90 and 92 in Figures 1 & 3 of Andresen are a statistics circuit having an input to accept the first bit value from the non-casual circuit

Data/Error Detectors 24, an input to accept the stream of corrected data bits from the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96, and an output to supply threshold values to the multi-threshold circuit Amplitude Sense and Data Gates 20 in Figures 1 & 3 in response to analysis of the FEC error statistics).

The Examiner asserts that Exclusive OR circuit 112 in Figure 6 of Andresen is substantially a comparator since it provides a 1 if input signal match and a 0 if they do not match. Exclusive OR circuit 112 in Figure 6 receives a current bit estimate A and a previous bit estimate A from Delay 110 in Figure 6. Previous bit estimate A from Delay 110 in Figure 6 is a bit value for a non-current clock cycle. Hence Andresen teaches an output DATA in Figure 1 of Andresen to supply a first bit value for a current clock cycle in response to comparing a first bit estimate A for the current clock cycle, to bit values determined A from Delay 110 in Figure 6 in a non-current clock cycle (Note Figure 6 is the Data Detector 28 of Figure 1 in Andresen).

However Andresen does not explicitly teach the specific use of non-return to zero NRZ. The Authoritative Dictionary of IEEE Standards Terms defines NRZ as a modulation technique for magnetic tape as taught in Andresen. The Examiner would like to point out that NRZ is a modulation technique to improve readability of a magnetic medium. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Andresen with the teachings of The Authoritative Dictionary of IEEE Standards Terms by including use of non-return to zero NRZ. This modification would have been obvious to one of ordinary skill in the art, at the time the

invention was made, because one of ordinary skill in the art would have recognized that use of non-return to zero NRZ would have improved readability of a magnetic medium. However Andresen does not explicitly teach the specific use of FEC error statistics to set the threshold.

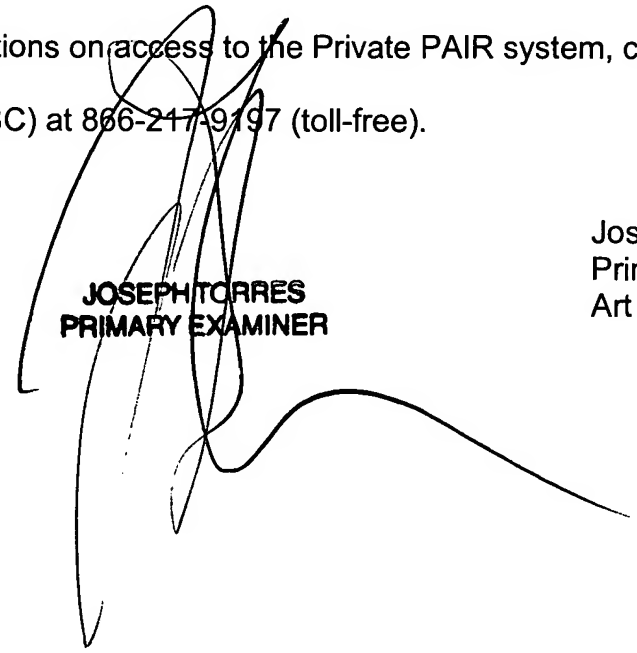
Abe, in an analogous art, teaches use of FEC error statistics to set the threshold. Figure 37 of Abe teaches BER CALC circuit for producing error statistics for use in threshold adjusting circuit 2604. Note: Abe teaches that Figure 37 is a modification of Figure 33 in Abe using BER in order to equalize BER's for respective different symbol states (col. 36, lines 27-29 in Abe).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Andresen with the teachings of Abe by including use of non-return to zero NRZ. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of non-return to zero NRZ would have provided the opportunity to apply the teachings in the Andresen patent to a specific type of data for which it was designated such as NRZ which is a widely used form of encoding for magnetic storage devices in order to equalize BER's for respective different symbol states (col. 36, lines 27-29 in Abe).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133